# ECS Configuration Change Request



| 1. Originator | 2. Log Date: | 3. CCR #: | 4. Rev: | 5. Tel: | 6. Rm #: | 7. Dept. |
|---|---|---|---|---|---|---|
| Sarah Lewallen | **10/11/02** | 02-0896 | | 301-925-0865 | 2117B | SE |

**8. CCR Title:** Add 8 CPUS each to g0spg01 and g0spg07

| 9. Originator Signature/Date | 10. Class | 11. Type: | 12. Need Date: |
|---|---|---|---|
| **Sarah Lewallen /s/ 10/10/02** | **II** | **CCR** | 11/15/02 |

| 13. Office Manager Signature/Date | 14. Category of Change: | 15. Priority: (If "Emergency" fill in Block 27). |
|---|---|---|
| **James Mather /s/ 10/10/02** | Update ECS Baseline Doc. | Routine |

| 16. Documentation/Drawings Impacted *(Review and submit checklist):* | 17. Schedule Impact: | 18. CI(s) Affected: |
|---|---|---|
| 920-TDG-001 | None | SPRHW |

| 19. Release Affected by this Change: | 20. Date due to Customer: | 21. Estimated Cost: |
|---|---|---|
| 6A, 6B | | None - Under 100K |

**22. Source Reference:** ☐ **NCR (attach)** ☐ **Action Item** ☐ **Tech Ref.** ☐ **GSFC** ☒ **Other:**
Available hardware

**23. Problem: (use additional Sheets if necessary)**
Additional CPUs would help with the SSIT processing on g0spg01 and g0spg07

**24. Proposed Solution: (use additional sheets if necessary)**
CPUs for Challenge systems have become available as machines have been retired. Reuse these CPUs to add 8 CPUs to each g0spg01 and g0spg07.
g0spg01 - CVM774 and CSL290
g0spg07 - EPD212 and CTJ733

**25. Alternate Solution: (use additional sheets if necessary)**
Leave as is.

**26. Consequences if Change(s) are not approved: (use additional sheets if necessary)**
None

**27. Justification for Emergency (If Block 15 is "Emergency"):**

**28. Site(s) Affected:** ☐ EDF ☐ PVC ☐ VATC ☐ EDC ☒ GSFC ☐ LaRC ☐ NSIDC ☐ SMC ☐ AK ☐ JPL ☐ EOC ☐ IDG Test Cell ☐ Other

| 29. Board Comments: | 30. Work Assigned To: | 31. CCR Closed Date: |
|---|---|---|
| | | |

| | |
|---|---|
| **32. EDF/SCDV CCB Chair (Sign/Date):** | **Disposition:** Approved App/Com. Disapproved Withdraw Fwd/ESDIS ERB Fwd/ECS |
| **33. M&O CCB Chair (Sign/Date):** **Gary Gavigan /s/ 10/15/02** | **Disposition:** Approved App/Com. Disapproved Withdraw Fwd/ESDIS ERB Fwd/ECS |
| **34. ECS CCB Chair (Sign/Date):** | **Disposition:** Approved App/Com. Disapproved Withdraw Fwd/ESDIS ERB Fwd/ESDIS |

# ADDITIONAL SHEET

**CCR #:** **Rev:** **Originator:** Sarah Lewallen

**Telephone:** 301-925-0865 **Office:** 2117B

**Title of Change:**

g0spg01 - has slot 9 and 14 available
Main memory size: 2048 Mbytes, 8-way interleaved
slot 1 - MC3 Memory Board 512 MB of memory
Bank A contains 64 MB SIMMS (Enabled)
Bank B contains 64 MB SIMMS (Enabled)
slot 2 - MC3 Memory Board 512 MB of memory
Bank A contains 64 MB SIMMS (Enabled)
Bank B contains 64 MB SIMMS (Enabled)
slot 3 - MC3 Memory Board 512 MB of memory
Bank A contains 64 MB SIMMS (Enabled)
Bank B contains 64 MB SIMMS (Enabled)
slot 4 - MC3 Memory Board 512 MB of memory
Bank A contains 64 MB SIMMS (Enabled)
Bank B contains 64 MB SIMMS (Enabled)
slot 5 - 4xR10 with 2MB secondary cache
slot 6 - 4xR10 with 2MB secondary cache
slot 7 - 4xR10 with 2MB secondary cache
slot 8 - 4xR10 with 1MB secondary cache
slot 9 - available
slot 10 - 4xR10 with 2MB secondary cache
slot 11 - IO4 revision 1
slot 12 - 4xR10 with 2MB secondary cache
slot 13 - IO4 revision 1
slot 14 - available
slot 15 - IO4 revision 1

g0spg07 - has slots 6, 9, and 11 available
Main memory size: 4096 Mbytes, 8-way interleaved
slot 1 - MC3 Memory Board 1024 MB of memory
Bank A contains 64 MB SIMMS (Enabled)
Bank B contains 64 MB SIMMS (Enabled)
Bank C contains 64 MB SIMMS (Enabled)
Bank D contains 64 MB SIMMS (Enabled)
slot 2 - MC3 Memory Board 1024 MB of memory
Bank A contains 64 MB SIMMS (Enabled)
Bank B contains 64 MB SIMMS (Enabled)
Bank C contains 64 MB SIMMS (Enabled)
Bank D contains 64 MB SIMMS (Enabled)
slot 3 - MC3 Memory Board 1024 MB of memory
Bank A contains 64 MB SIMMS (Enabled)
Bank B contains 64 MB SIMMS (Enabled)
Bank C contains 64 MB SIMMS (Enabled)
Bank D contains 64 MB SIMMS (Enabled)
slot 4 - MC3 Memory Board 1024 MB of memory
Bank A contains 64 MB SIMMS (Enabled)
Bank B contains 64 MB SIMMS (Enabled)
Bank C contains 64 MB SIMMS (Enabled)
Bank D contains 64 MB SIMMS (Enabled)
slot 5 4xR10 with 1MB secondary cache
slot 6 - available

slot 7 - 4xR10 with 2MB secondary cache
slot 8 - 4xR10 with 1 MB secondary cache
slot 9 - available
slot 10 - 4xR10 with 2MB secondary cache
slot 11 - available
slot 12 - 4xR10 with 2MB secondary cache
slot 13 - IO4 revision 1
slot 14 - 4xR10 with 2MB secondary cache
slot 15 - IO4 revision 1